## **REMARKS**

Claims 1-8 are pending in the application.

Claims 1-8 have been rejected.

Claims 1-2 and 4-8 have been amended, as set forth herein.

Claim 3 has been canceled, without prejudice.

## I. REJECTION UNDER 35 U.S.C. § 102

Claims 1, 2 and 4-8 were rejected under 35 U.S.C. § 102(b) as being anticipated by Gu (US Patent No. 6,173,009). The rejection is respectfully traversed.

A cited prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131; *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). Anticipation is only shown where each and every limitation of the claimed invention is found in a single cited prior art reference. MPEP § 2131; *In re Donohue*, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985).

Without conceding that each and every element recited in original independent Claims 1 and 4 are disclosed by Gu, 1 to further prosecution, Applicant has amended independent Claims 1 and 4 to include the elements recited in dependent Claim 3. The Office Action concedes that Gu does not disclose or describe these elements.

Accordingly, the Applicant respectfully requests the Examiner withdraw the § 102(b) rejection of Claims 1-2 and 4-8.

## II. REJECTION UNDER 35 U.S.C. § 103

Claim 3 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Gu (US Patent No. 6,173,009). The rejection is respectfully traversed.

<sup>&</sup>lt;sup>1</sup> For example, Gu does not appear to describe that the transition matrix T (whether raised to a power) is decomposed into two matrices, as recited in independent Claims 1 and 4.

In ex parte examination of patent applications, the Patent Office bears the burden of establishing a prima facie case of obviousness. MPEP § 2142; In re Fritch, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992). The initial burden of establishing a prima facie basis to deny patentability to a claimed invention is always upon the Patent Office. MPEP § 2142; In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Piasecki, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984). Only when a prima facie case of obviousness is established does the burden shift to the applicant to produce evidence of nonobviousness. MPEP § 2142; In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Rijckaert, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). If the Patent Office does not produce a prima facie case of unpatentability, then without more the applicant is entitled to grant of a patent. In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Grabiak, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985).

A prima facie case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. In re Bell, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993). To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. MPEP § 2142. In making a rejection, the examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), viz., (1) the scope and content of the prior art; (2) the differences between the prior art and the claims at issue; and (3) the level of ordinary skill in the art. In addition to these factual determinations, the examiner must also provide "some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." (In

re Kahn, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir 2006) (cited with approval in KSR Int'l v. Teleflex Inc., 127 S. Ct. 1727, 1741, 82 USPQ2d 1385, 1396 (2007)).

Gu describes a circuit that is designed to receive a plurality of index signals. The circuit includes a memory circuit arranged to store a plurality of state vectors. A multiplex circuit is coupled to the memory circuit wherein the multiplex circuit selectively produces one of the state vectors in response to at least one of the index signals. A matrix generator circuit is arranged to produce a variable matrix in response to at least another of the index signals. Moreover, a logic circuit is coupled to the multiplex circuit and the matrix generator circuit. The logic circuit is arranged to produce a logical combination of the variable matrix and said one of the state vectors. Gu, Abstract.

One of the objects of the claimed invention is to overcome the shortcomings of configurable multi-step linear feedback shift registers because the amount of time needed to generate the output can be reduced significantly (Applicant's Specification, p. 4, lines 23-25). As described in the present application, the state vector can be multiplied by the state transition matrix to the power of W (multiple state transition matrix) instead of multiplying the state vector by the state transition matrix W times (Applicant's Specification, p. 3, lines 1-7). If the state transition matrix is represented by F, then a W-step LFSR entails multiplication of the state vector by F<sup>W</sup>. This approach leads to an acceptable clock cycle time, but additional circuitry (such as AND/XOR gates) may be needed to compute F<sup>W</sup>. The additional hardware provides for the evaluation of the large number of complex expressions in F<sup>W</sup>. A goal of Applicant's claimed invention is to minimize the clock cycle time while also minimizing the amount of additional hardware required to compute the next state of the LFSR. This may be achieved by the additional claim language added by this amendment in independent Claims 1 and 4.

Gu describes Boolean minimization of transition matrices, but is silent with respect any disclosure or description of the first and second matrices and their elements (and that the two matrices are decomposed from the transition matrix to the power of W) – as recited in amended Claims 1 and 4. Hence, the elements of these matrices are neither explicitly nor implicitly described in Gu. The Office Action points to Col. 4, line 32 through Col. 5, line 67 in Gu as

disclosing "defining matrix elements used in the [sic] LFSR circuit producing state transitions." Because of this, the Office Action argues, it would be obvious "to use the matrices implemented in the circuit, as taught by Gu, for the benefit of obtaining the predicable result of state transitions." Office Action, page 4.

To make out a prima facie case of obviousness, the prior art reference (or references when combined) must teach or suggest <u>all</u> the claim limitations. The Gu reference simply does not disclose, teach or suggest the elements of the first and second matrices as recited in amended independent Claims 1 and 4, and further, Gu fails to disclose, teach or suggest that the state transition matrix to the power of W is decomposed into these two matrices. See, Claims 1 and 4.

Therefore, Applicant respectfully submits that the Office Action has not established, and cannot establish, a prima facie case of obviousness based on the Gu reference for amended independent Claims 1 and 4.

## III. CONCLUSION

As a result of the foregoing, the Applicant asserts that the remaining Claims in the Application are in condition for allowance, and respectfully requests an early allowance of such Claims.

ATTORNEY DOCKET NO. NL 030348 (STNX01-30348)
U.S. SERIAL NO. 10/552,048
PATENT

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *rmccutcheon@munckcarter.com*.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

MUNCK CARTER, P.C.

Date:  $\sqrt{5/200}$ 

Robert D. McCutcheon Registration No. 38,717

P.O. Box 802432 Dallas, Texas 75380 (972) 628-3632 (direct dial) (972) 628-3600 (main number)

(972) 628-3616 (fax)

E-mail: rmccutcheon@munckcarter.com